introspect technology

DATASHEET

SV7M-DDRPA DDR/LPDDR Protocol Analyzer

M SERIES

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Introduction

The SV7M-DDRPA is a solution for validating and debugging DDR5 and LPDDR5 memory interfaces. For LPDDR5 DRAM applications, this analyzer can capture read and write commands and data bursts, and it is able to provide deep analysis of all protocol events on the LPDDR5 bus. Coupled with a Remote Sampling Head (RSH) solution, the SV7M-DDRPA is ideal for measuring LPDDR5 components. This document introduces the analyzer and illustrates the usage of the Remote Sampling Heads.

Hardware

Figure 1 shows the three main hardware components. These are:

- The SV7M-DDRPA
- Remote Sampling Heads (RSH)
- Interposer solution for embedded and formfactor applications

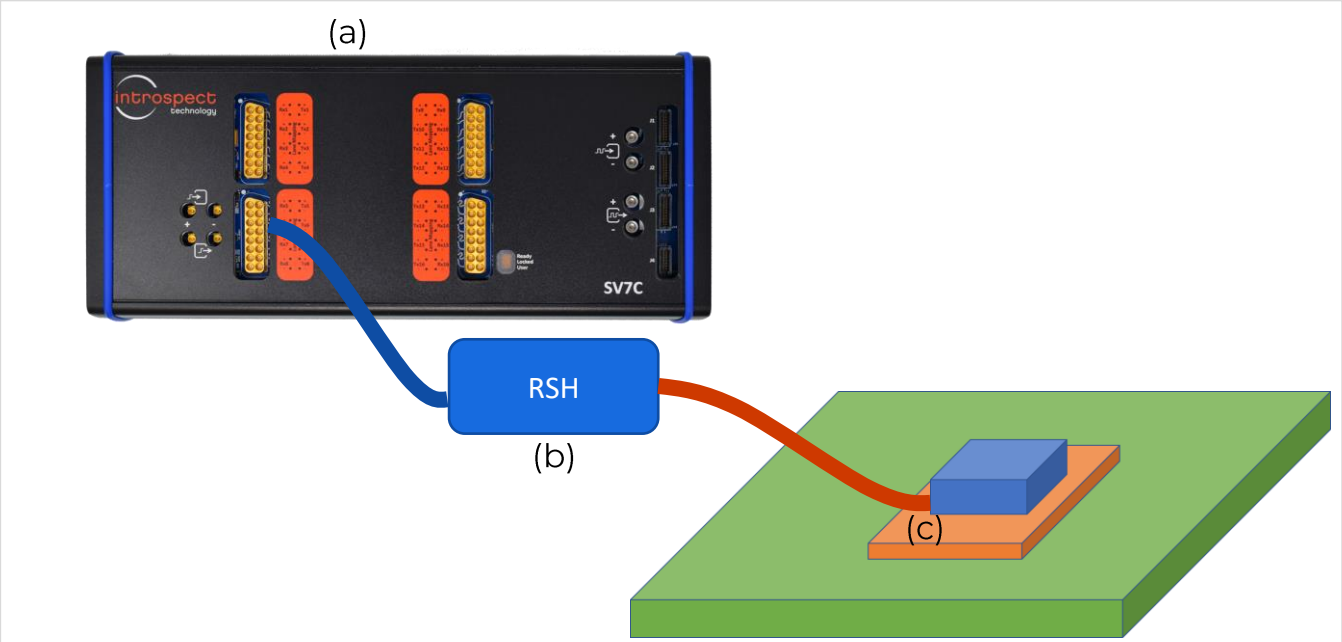

Figure 1: Illustration of the three main hardware components of an LPDDR5 probing system.

REMOTE SAMPLING HEADS

By deploying active probe technology, the Remote Sampling Heads ensure reliable sampling of data at the maximum transfer speed of LPDDR5. They provide a miniature coaxial cable interface on the side of the device under test (connected through an I-PEX connector) and a coaxial cable interface on the side of the protocol analyzer. In addition to being used in conjunction with the SV7M-DDRPA, the Remote Sampling Heads also support direct connection to an oscilloscope. Figure 2 shows how the Remote Sampling Head enables probing live traffic with a real device.

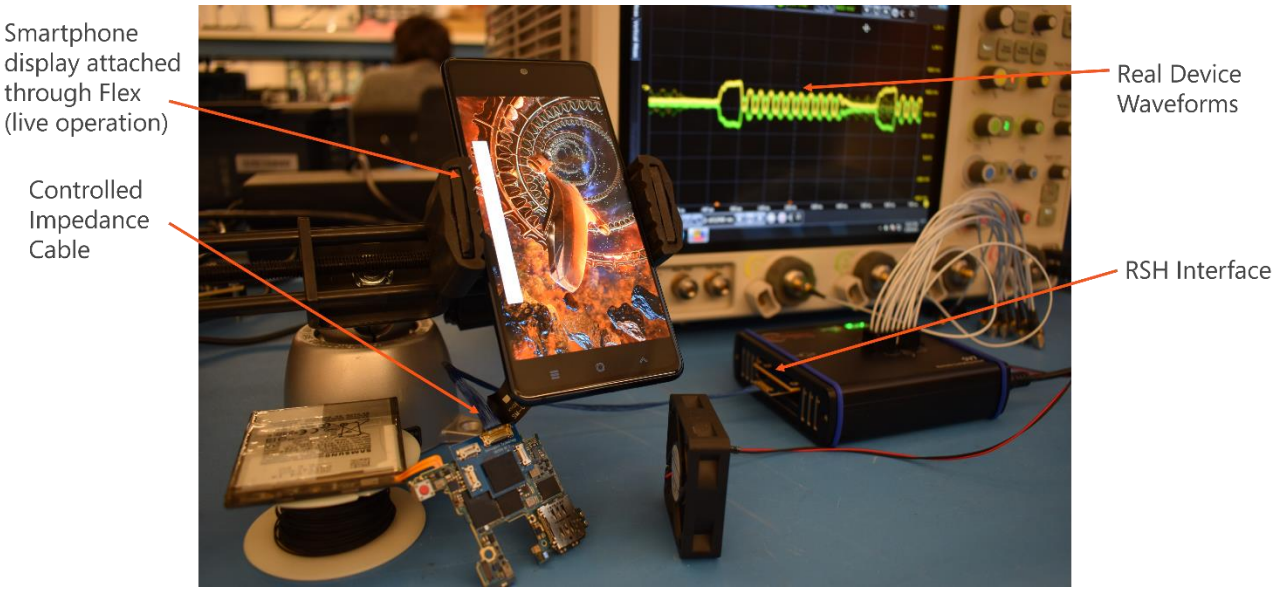

Figure 2: Illustration of the Remote Sampling Head connections.

INTERPOSER

The LPDDR5 interposer solution provides access to the full command and data bus for one channel. Figure 3 below shows the components that make up the interposer solution.

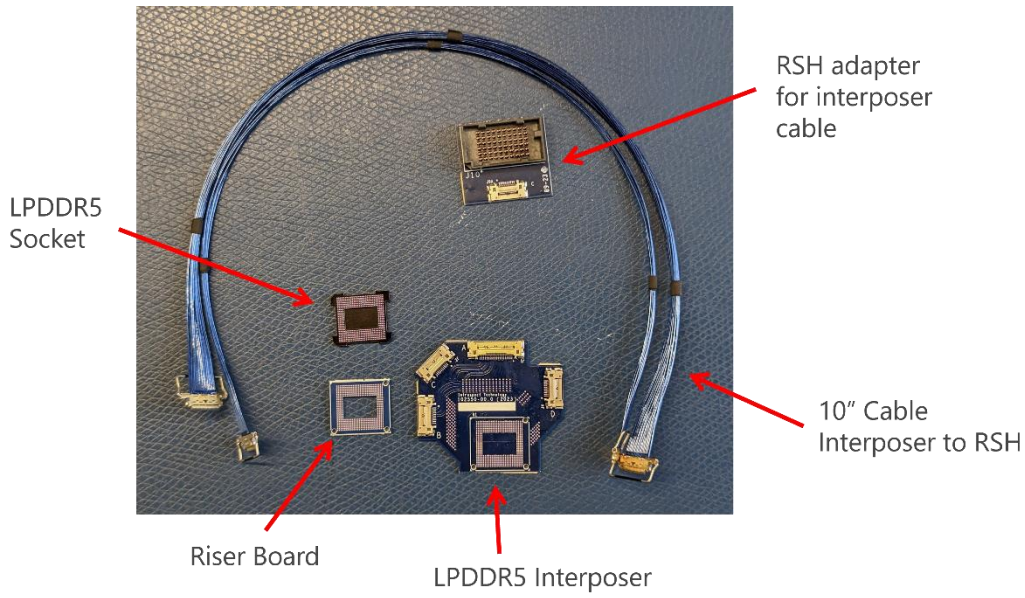

Figure 3: LPDDR5 Interposer.

Interposers are available for the following package types:

- 496 ball LPDDR5 Package on Package
- 315 ball LPDDR5 Standard Package
- 441 ball LPDDR5 Standard Package
- 78 ball DDR5 Standard Package

Please contact Introspect Technology for more information as additional packages may be available on request.

Features

SUMMARY SPECIFICATIONS OF THE SV7M-DDRPA FOR LPDDR5

TABLE 1

PARAMETER	VALUE	UNITS	DESCRIPTION AND CONDITIONS
Ports			
Number of high-speed receivers	32		Divided over two SV7C instruments, each providing 16 channels
Number of GPIO pins	12		Can be used for triggering and low-speed control
Number of I2C master ports	1		SV7M-DDRPA can be used to program slave devices through Python
Connections to PC for the Pinetree software control	2		USB Type-C
Physical Layer Characteristics			
Maximum synchronous data rate	28	Gbps	Sampling rate of the tester
Maximum asynchronous data rate	56	Gbps	Sampling rate of the tester
Memory			
Per-receiver capture memory	268,435,456	Bytes	Per pin capture buffer depth
Comparator Performance			
Minimum Threshold Voltage	-400	mV	
Maximum Threshold Voltage	+400	mV	
Threshold Voltage Resolution	20	mV	
Threshold Voltage Accuracy	>15% or 15 mV	%, mV	
Minimum Detectable Differential Voltage	90	mV	

Maximum Allowable Differential Voltage	1200	mV	
Resolution Enhancement			
DC Gain Settings	0, 3, 6, 8, 10	dB	
CTLE High Frequency Settings	0 … 15	dB	
DC Gain Settings	Per Lane		
CTLE Settings	Per Lane		
Timing Generator Performance			
Timing Resolution	7.8125	mUI	Measured at 28 Gbps
Range	Unlimited		
LPDDR5 DUT Characteristics			
Temperature testing range	0-50	C	
Voltage specification	0.3-0.6	V	VDDQ range

TIMING ANALYSIS

In-depth timing analysis is performed on all command captures based on the LPDDR5 specification. Table 2 below shows a summary of the timing measurements available for LPDDR5 command captures. This list is provided as an example and is not exhaustive.

SUMMARY OF LPDDR5 TIMING ANALYSIS

TABLE 2

TIMING CATEGORY	DETAILS	EXAMPLES
Active command-to-command timings	Spec sections 7.3.1, 8.2, 8.3, 9.2	tRTW, tRCD, tRP, tWR, tWTR, tRBTP, tAAD, tFAW, tRRD, tPPD, tRC, tRAS
Mode register access command-to-command timings	Spec table 252	tMRR, tMRW, tMRD, tMRRI
Refresh command timings	Spec section 7.5.2	tREFW, tREFI, tRFM
Illegal command sequences		• MRW1 not followed by MRW2 • ACT1 not followed by CAS/WR/RD/MWR/MRR/PRE/ACT2 • PRE followed by WR/RD to same bank

Revision Number	History	Date
1.0	Document Release	May 12, 2021
1.1	Updated Product Name and Descriptions	September 22, 2021
1.2	Updated RSH configuration and added section on capture triggering and protocol decode	February 24, 2022
1.3	Divided information into Hardware and Features sections. Added photos for RSH and interposer. Updated screen shots for protocol analysis and added details. Updated specifications table.	February 28, 2025
1.4	Updated specifications tables.	March 4, 2025
1.5	Removed LPDDR5 Protocol Analysis subsection (moved it to the Quick Start Guide)	October 8, 2025

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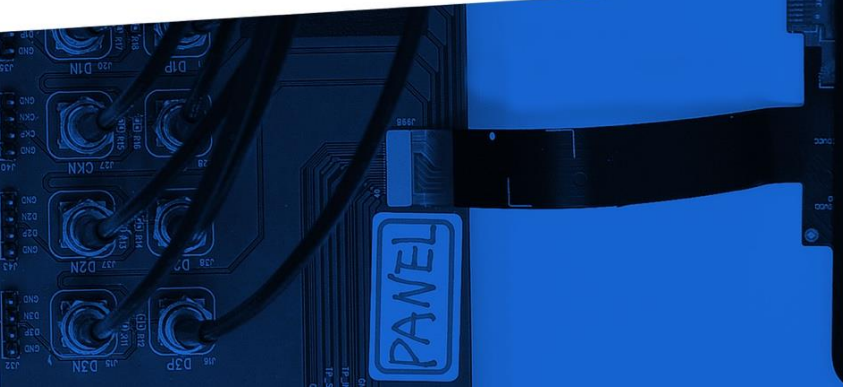

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